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A NEW THREE PHASE 5-LEVEL CONVERTER BY CASCADING A FLYING CAPACITOR INVERTER AND AN H-BRIDGE

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ABSTRACT

Multilevel converters have been widely used in motor drive applications for the advantages of high-power capacity, low total harmonic distortion, low switching frequency, and so. As an answer to the increasing demand for drives which can increase the power factor and reduce the switching frequency, the five-level converter has come into being. The five-level neutral-point-clamped (5L-NPC) converter and the five-level floating-capacitor (5L-FC) converter are both the expansions of typical three-level topologies. However, both of them have the difficulty in balancing the voltages of capacitors. The voltage balancing can affect in producing the desire voltage levels of the inverter. Hence the performance of the such inverters are been highly depended up on the voltage balancing schemes. To overcome the issues , a new three-phase, five-level inverter topology with a single-dc source is presented. The proposed topology is obtained by cascading a three-level flying capacitor inverter with a flying H-bridge power cell in each phase. This topology has redundant switching states for generating different pole voltages. By selecting appropriate switching states using SVPWM, the capacitor voltages can be balanced instantaneously (as compared to the fundamental) in any direction of the current, irrespective of the load power factor. Another important feature of this topology is that if any H-bridge fails, it can be bypassed and the configuration can still operate as a three-level inverter at its full power rating. Simulation results are obtained using MATLAB/ Simulink environs for value of the study.

Index Terms- Flying capacitor (FC), H-bridge, multilevel inverter, space vector pulse width modulation (SVPWM).

1. INTRODUCTION

Traditional inverters are voltage-source inverter and current-source inverter since, multilevel inverters (MLI)have been receiving much attention and as a result many different topologies have been proposed. The academic papers and theses focusing on MLI topologies are almost innumerable. These MLI topologies can be classified according to many criteria. This paper will focus on three-phase multilevel inverters.

The five-level neutral-point-clamped (5L-NPC) converter and the five-level floating-capacitor (5L-FC) converter are both the expansions of typical three-level topologies. [1].For single-phase MLI, the most common topologies are the cascaded, diode-clamped, and capacitor clamped types [2]– [3]. There occur many
other topologies [4]–[26]. In general, MLI topologies can be classified into two types: Type I and Type II. Type I uses numerous dc voltage sources and Type II uses numerous (split or clamping) dc voltage capacitors. Type I includes the conventional cascaded topologies [1]–[3], those presented in [4]–[8] and so forth. Type II includes the traditional diode-clamped, capacitor-clamped inverters, the topologies proposed in [9]–[26]. In terms of single phase multilevel inverters, the disadvantages of the two types are obvious. Type I suffers from the

availability of the numerous dc voltage sources. In practice, bulky transformers either of low or medium frequency are usually necessary if a Type I inverter is elected. The problem with Type II is mainly the balancing of the dc capacitor voltages, though some MLI topologies can achieve self-balancing with certain control algorithms.

The multilevel CHB inverter with isolated supplies presented in [27] has many advantages compared to the NPC and FC topologies. The CHB configuration does not require clamping diodes and the input power is distributed among different input sources that makes it more suitable for certain applications [2]. One additional advantage of the CHB converter is that if any device fails in the H-bridges, the inverter can still be operated at reduced power level and, hence, this configuration is fault tolerant to some extent [27], [28].

A level-shifted carrier pulse width modulation (PWM) with a dc-offset injection method was proposed to control the neutral point voltage for a five-level FC-based ANPC converter [6].The redundant switching states are utilized to control the voltages across the FCs. The behaviour of the neutral-point voltage and current for the three-level ANPC converter, the five-level FC-based ANPC converter, and the SMC converter was demonstrated with graphical representation for various modulation techniques in [16]. The five-level virtual-flux direct power control for the five-level ANPC converter was implemented in [18].

Three phase voltage-fed PWM inverters are in lately times showing growing fame for multi-megawatt industrial drive applications. The main reasons for this esteem are easy sharing of large voltage between the series devices and the amendment of the harmonic quality at the output as compared to a two level inverter. In the inferior end of power, GTO devices are being replaced by MOSFET's because of their rapid evolution in voltage and current ratings and higher switching frequency.

The model of A Three phase 5-Level inverter is discussed based on space vector theory for adjustable speed drives. Simulation results are obtained using MATLAB/Simulink environs for value of the study.

2. PROPOSED THREE-PHASE FIVE-LEVEL INVERTER

Fig. 1 shows the circuit of the proposed three-phase five level inverter. In Fig. 1, V_{dc1} is the dc-link. and FC voltage equal to Vdc/2, which can generate voltages of 0, Vdc/2, and Vdc with respect to point 0. A capacitor-fed H-bridge is cascaded to each phase of the inverter. The voltage across the H-bridge capacitor has to be maintained at Vdc/4. The switching states of the useful voltage levels and their effects on the capacitor voltages based on the current direction.

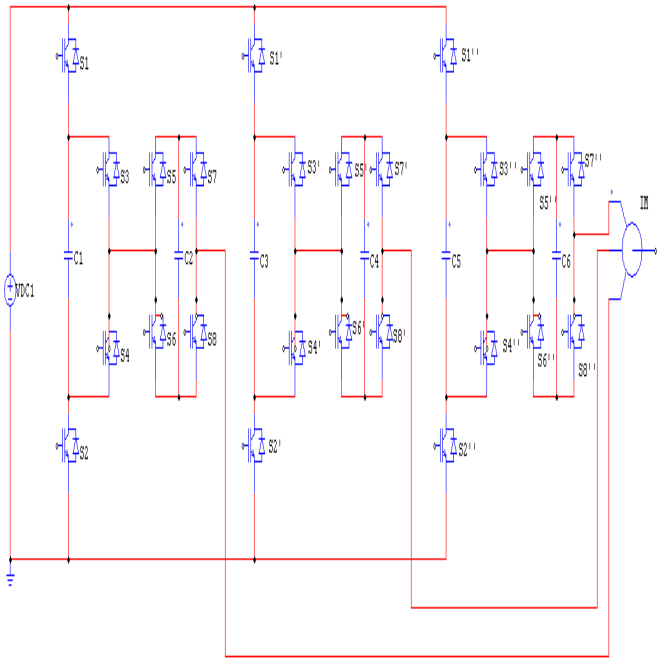

Fig.1. Proposed Three-phase five-level inverter.

For voltage levels of Vdc/4 and Vdc3/4, there are three redundant states. By switching between these three states the capacitors C1 and C2 can be charged or discharged for any direction of the current. The voltage level of Vdc /2 has two redundant states. By switching between them, C1 can be charged or discharged based on the current direction. When Vdc /2 is applied, the C2 is not affected. As the capacitors can be either charged or discharged by switching between the redundant states, based on the current direction, quick capacitor voltage balancing is possible, irrespective of the load power factor. To maintain the capacitor voltages at a fixed value, the capacitor voltages are sampled at regular intervals and a hysteresis controller is used to switch between the redundant states based on the current direction to balance the capacitor voltages. Each pole can generate one of the five voltage levels 0, Vdc /4, Vdc /2, 3 Vdc /4, and Vdc. The effective voltage space vector formed based on the three-phase pole voltages is given by $VSV = VAO + VBO\_ 120\circ - VCO\_ 120\circ$(1)

3. PROPOSED MODULATION METHOD SPACEVECTOR MODULATION (SVM)

The SVM is a classy, averaging algorithm which gives 15% more voltage output compared to the Sinusoidal PWM algorithm, thereby rising the Vdc utilization. It also reduces the THD as well as switching loss. Like Sinusoidal PWM, the SVM is similarly a scalar control. The three-phase line-to-neutral sine waves required for driving the 3-phase induction motor can be represented as 120° phase-shifted vectors .

For a balanced 3-phase system, these vectors add to zero. Therefore, they can be expressed as a single space reference vector. By controlling the amplitude and the frequency of reference vector, the motor voltage and the motor frequency can be precise. Hence, this algorithm is known as the SVPWM.

Any three time varying quantities, which always sum to zero and are spatially detached by 120° can be expressed space vector modulation concepts. As time rises, the angle of the space vector rises, causing the vector to spin with frequency equal to the frequency of the sinusoids. A three phase system defined by *Va(t), Vb(t), Vc(t)*) can be represented uniquely by a spinning vector,

$$V_a(t)+V_b(t)e^{j2\pi/3}+ V_c(t)e^{-j2\pi/3} \quad (1)$$

Where,

$$V_a(t) = V_m \sin\omega t$$

$$V_b(t) = V_m \sin(\omega t-2\pi/3)$$

$$V_c(t) = V_m \sin(\omega t+2\pi/3)$$

In space vector pulse width modulation technique, the three phase stationary reference frame voltages or each inverter switching state are charted to the complex two phase orthogonal α-β plane. The mathematical transmute for converting the stationary three phase parameters to the orthogonal plane is known as the Clark 's transformation. The reference voltage is signified as a vector in this plane. In a three-phase system, the vectorial illustration is achieved by the transformation given in Fig. 2.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (2)$$

where, (V_α,, V_β) are forming an orthogonal two phase system as $V = V_\alpha + jV_\beta$. In the three phase system, each pole voltage node can apply a voltage between $+V_{dc}/2$ and $-Vdc/2$. The principle of svpwm is based on the fact that there are only eight possible switching combinations

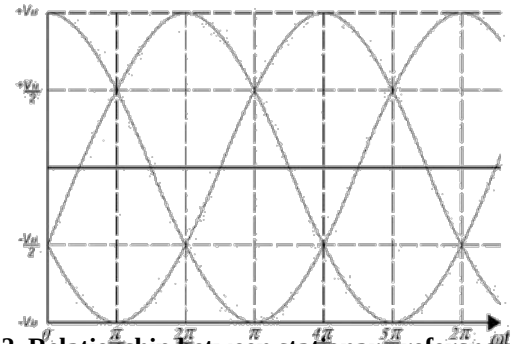

Fig.2. Relationship between stationary reference frame and α-β reference frame

Two of these states (V_0 and V_7) correspond to a short circuit on the output, while the other six can be considered to form stationary vectors in the α-β complex plane as shown in Fig. 3. The eight vectors are called the basic space vectors.

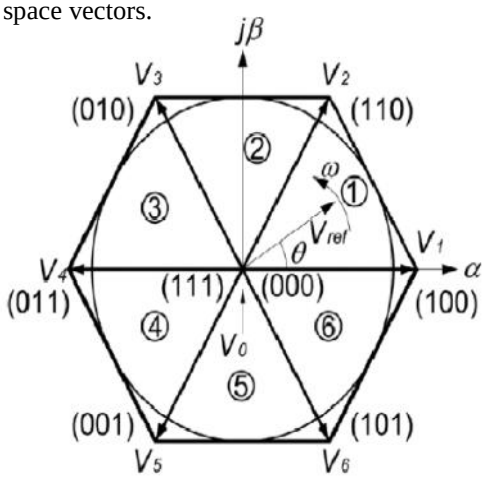

Fig.3. Reference vector as a geometric summing up of 2 nearest space vectors

the geometric summing up can be articulated mathematically as $V_{ref}= V_{ref}$angle θ

$$= \left(\frac{T_1}{T_s}\right).V_1 + \left(\frac{T_2}{T_s}\right).V_2 + \left(\frac{T_0}{T_s}\right).V_0 \quad (3)$$

where, T_1 is the time for which space vector V_1 is selected and T_2 is the time for which space vector V_2 is selected. The block diagram for generating SVM pulses is shown in Fig.6.

2. Identification of sector numbers

The six active-vectors are of equal magnitude and

are mutually phase displaced by $\pi/3$. The general articulation can be represented by,

$$V_n = V_{DC}.e^{j(n-1)\pi/3}, n = 1,2 \dots 6$$

3. Calculation of space vector duty cycle

The duty cycle calculation is done for each

triangular sector formed by two state vectors. The individual duty cycles for each sector boundary state vectors and the
zero state vector are given by,

$$\int_0^{Ts} Vref\ dt = \int_0^{T1} V1\ dt + \int_{T1}^{T2} V2\ dt + \int_{T1}^{T2} V0\ dt$$

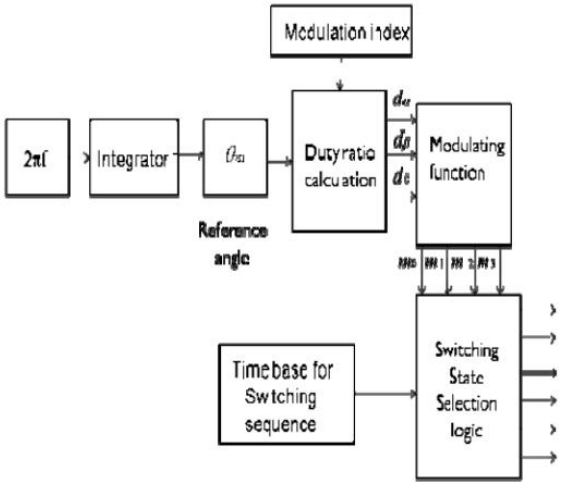

Fig.4. Block diagram f or SVPWM pulse generation

$$d_\alpha = \frac{V_{ref}}{V_{DC}}.[\sin((\pi/3) - \theta)]/\sin\pi/3 = m\sin((\pi/3) - \theta) \quad (8)$$

$$d_\beta = \frac{V_{ref}}{V_{DC}}.\{\sin\theta / [\sin\pi/3]\} = m\sin\theta \quad (9)$$

$$d_0 = 1 - d_{\alpha - d_\beta} \quad (10)$$

where,

$$d_\alpha = T_1/T_s,$$
$$d_\beta = T_2/T_s,$$
$$d_0 = T_0/T_s$$

This gives switching times T_0, T_1 and T_2 for each inverter state for a total switching period, T_s. Applying both active and zero vectors for the time periods given in (7) ensures that average voltage has the same magnitude as desired.

4. Calculation of modulating function

The four modulating functions, m_0, m_1, m_2 and m_3, in terms of the duty cycle for the space vector PWM scheme can be expressed as,

$$m_0 = d_0/2 \quad (11)$$

$$m_1 = m_o + d_\alpha \quad (12)$$

$$m_2 = m_1 + d_\beta \quad (13)$$

$$m_3 = m_0 + d_\beta \quad (14)$$

5. Initiation of SVPWM pulses

The required pulses can be initiated by comparing the modulating functions with t he triangular waveform. A symmetric seven segment technique is to alternate the null vector in each cycle and to contrary the sequence after each null vector. The switching pulse pattern for the 3 phases in the six sectors can be initiated. A typical seven segment switching sequence for generating reference vector in sector one is shown in Fig. 7.

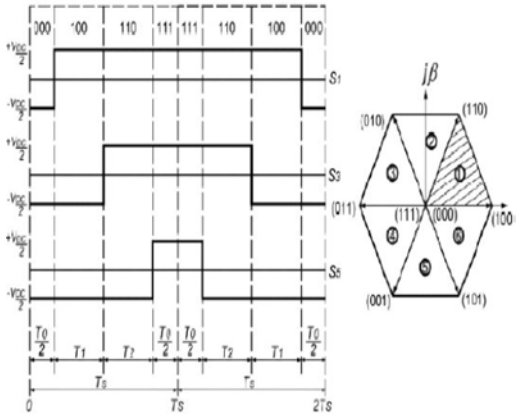

Fig.5. Switching logic signals

4. SIMULATION RESULTS

In order to verify the validity of the topology with the optimized modulation scheme in this paper, the intended inverter is tested with series-connected *RL* load. A three-phase inverter with a balanced star connected RL load is considered. A complete mathematical model of the SVPWM is developed and simulated using MATLAB/simulink to investigate the performance of a three phase inverter. Fig 8 shows the output voltage of 5-level inverter.

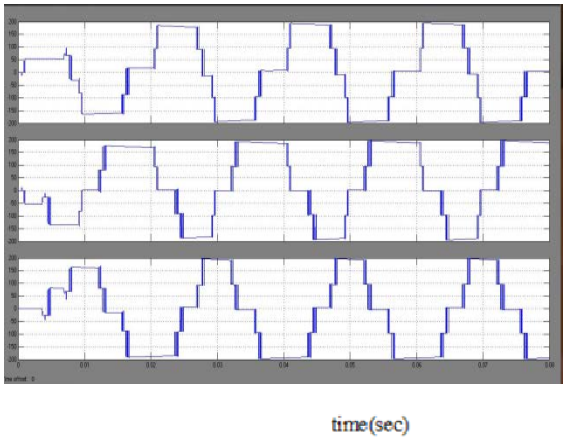

Fig.6. Output voltage of 5-level space vector PWM inverter

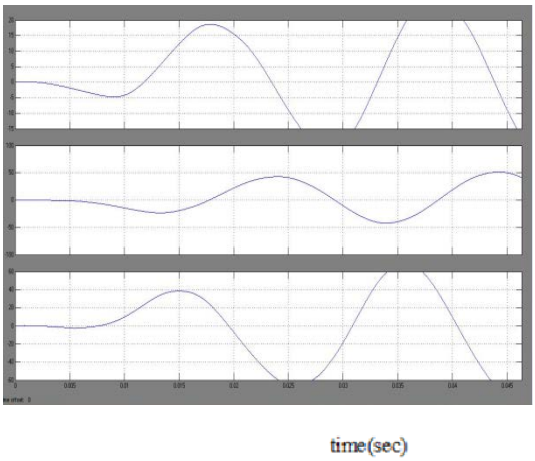

Fig.7. Output Current of 5-level space vector PWM inverter

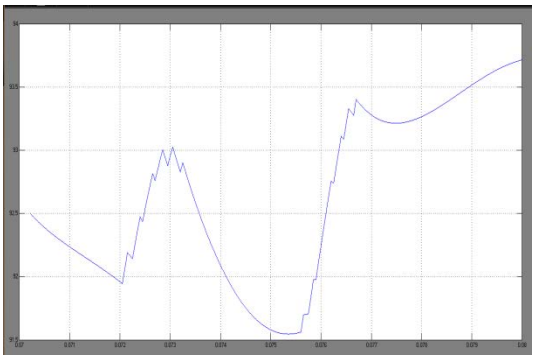

Fig.8. Efficiency of 5-level space vector PWM inverter

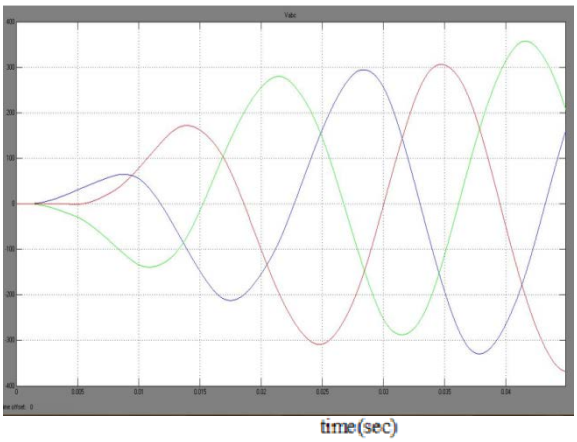

Fig.9. Three phase Output voltage of 5-level space vector PWM inverter

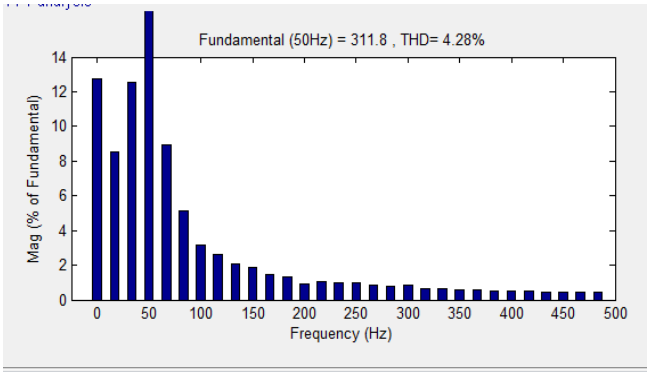

Fig.10. THD is comparably reduced to that of sin-PWM

5. CONCLUSION

In this paper, mathematical archetypal of a space vector modulated three phase inverter is originated and simulated using MATLAB/Simulink. Also Space Vector PWM is unique as compared to Sinusoidal pulse width modulation in many aspects like :

1) The Modulation Index (MI) is higher for SVPWM as compared to SPWM.

2) The output voltage is about 15% more in case of SVPWM as compared to Sin-PWM.

3) The current harmonics produced are much less in case of SVPWM.

With the increased output voltage, the user can sketch the motor control system with decreased current rating, which helps to decrease inherent conduction loss of the voltage source inverter. However despite all the above

mentioned advantages that SVPWM enjoys over Sin-PWM, SVPWM algorithm used in 3-level inverters is more complex because of large number of inverter switching states. Hence we see that there is a certain trade off that exists while using SVPWM for inverters for Adjustable speed Drive Operations. The key advantages of this topology compared to the conventional topologies include reduced number of devices and simple control.The main advantages of this topology are:

1) An important feature of this inverter is ability to balance capacitor voltages irrespective of load power factor.

2) Harmonics are less in the proposed work and fundamental THD was calculated.

3) Different voltage levels can be generated with less number of switches.

4) The Efficiency can be improved compared to the conventional type.

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